Tales From CDF Si Part XXX: The Data Acquisition System

and the latest headlines

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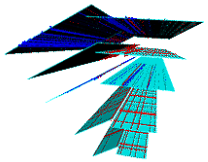
Fermi National Accelerator Lab.

FNAL Food For Thought, June 19th '01

Outline



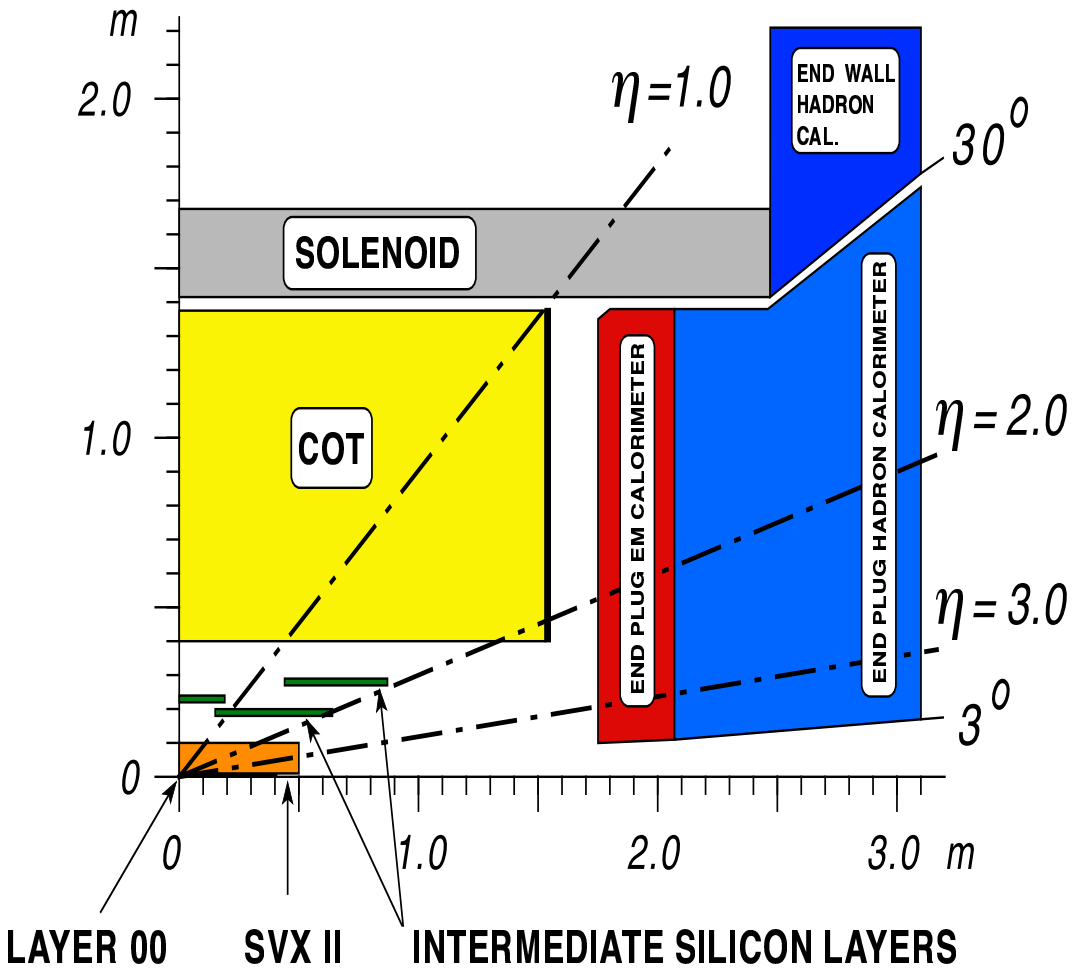
- Brief Overview of CDF Si (Oh No! Not Again!)
- The Silicon Data Acquisition System
  - It starts with a little chip
  - .. that hooks up to a Port Card
  - .. that is driven by a FIB
  - .. that sends its data to a VRB
  - .. all of which answers to an SRC
  - .. that talks to the CDF DAQ
  - .. and gives us tracks
- Pretty Pictures
- *TRACKS*
- Where are we now?

CDF II Si

SVXII: 3 barrels (90cm) with 5 layers of double sided silicon. 3 90^o and 2 small angle stereo layers. *60-140 μm pitch*

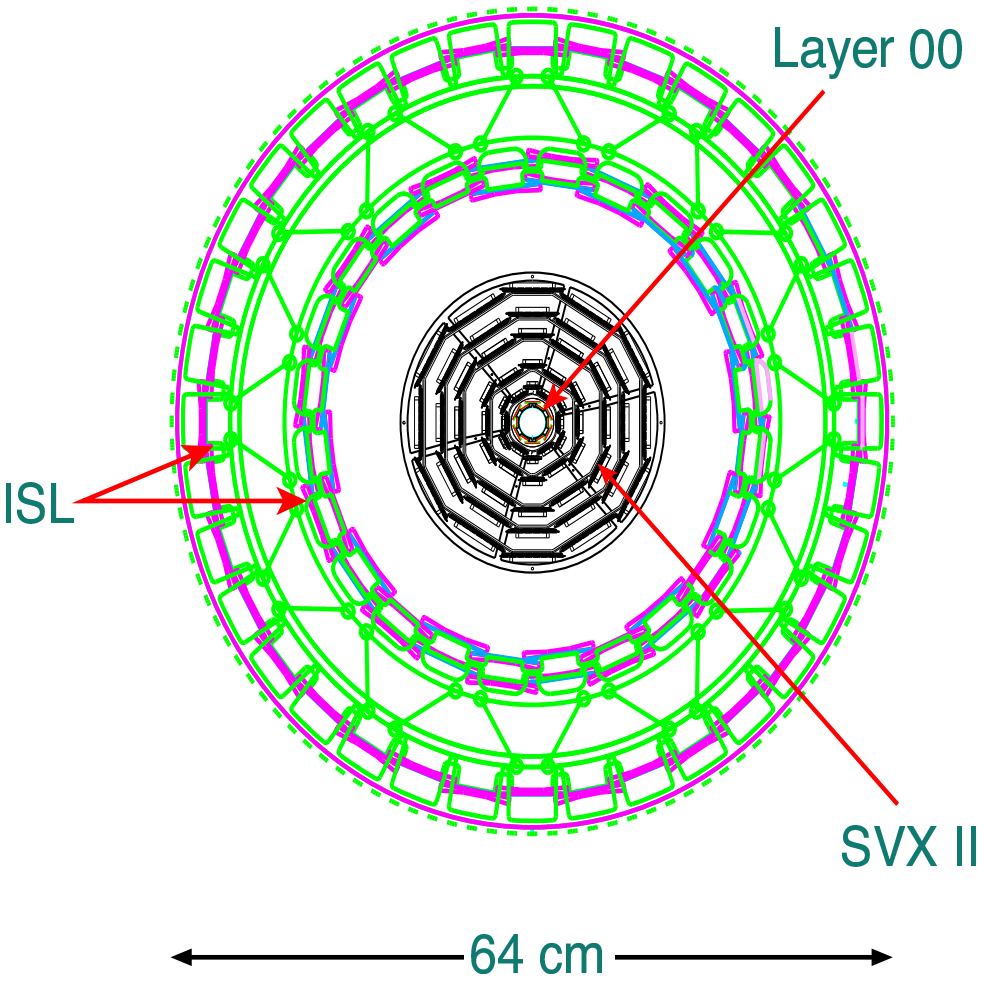
ISL: 1 layer of Si at $|\eta| < 1$, 2 layers at $1.0 < |\eta| < 2$. *112 μm pitch*

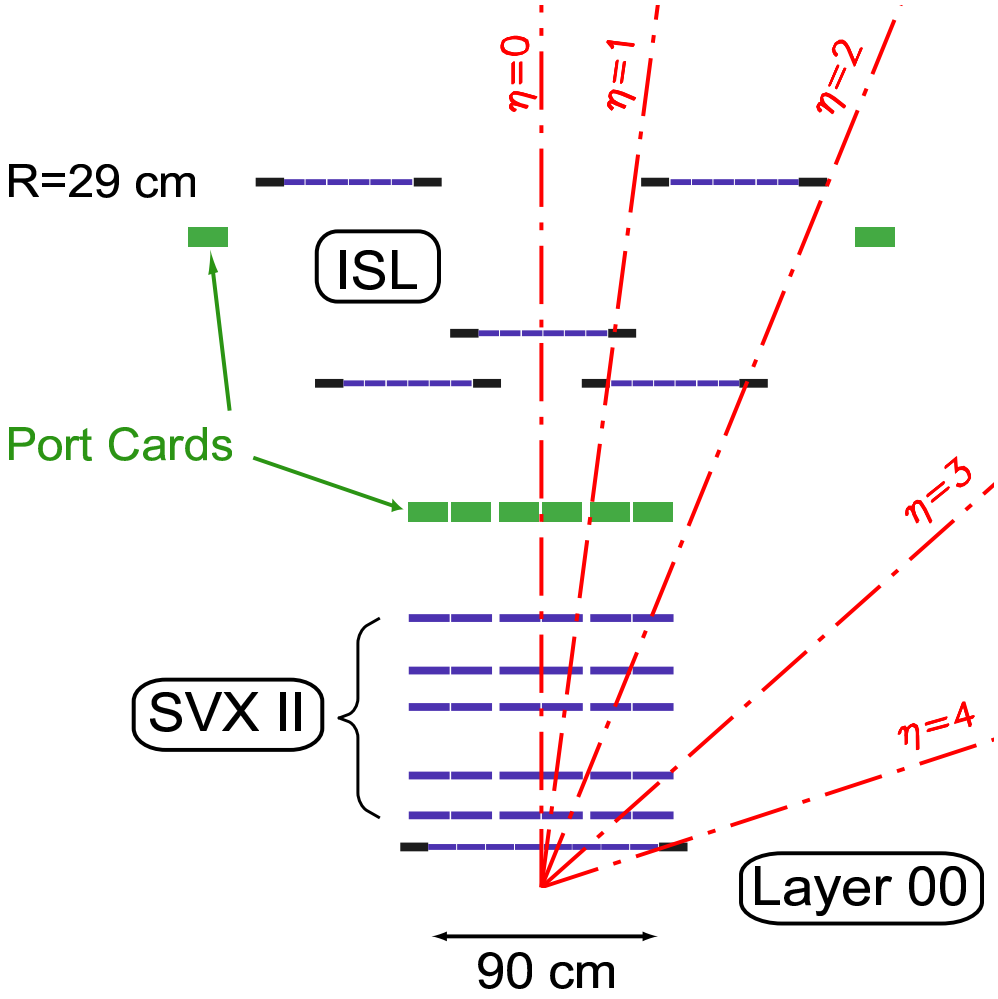
L00: Single sided Si layer on Be beam pipe. *50 μm pitch*



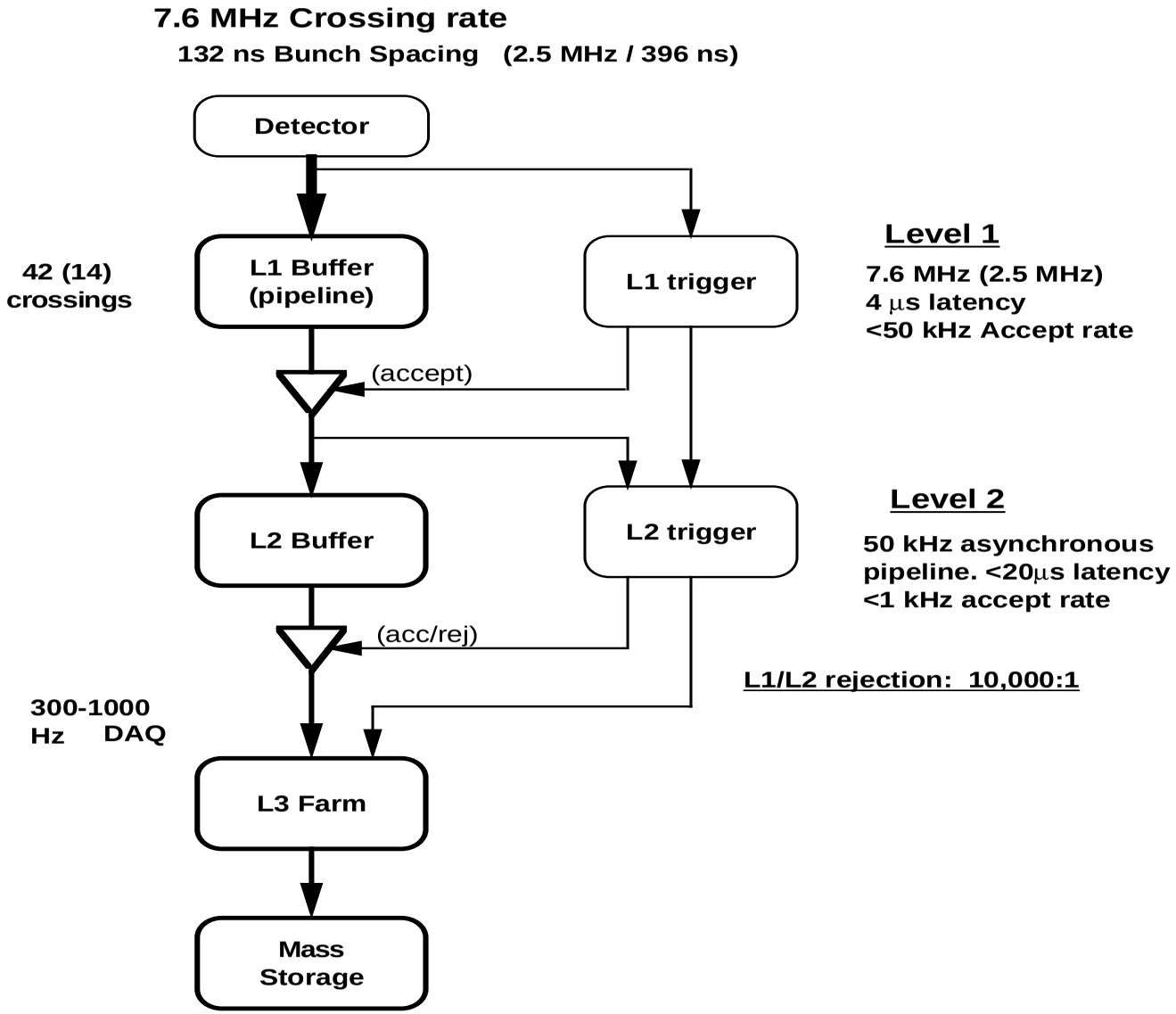
Over 700,000 readout channels.

Si Details

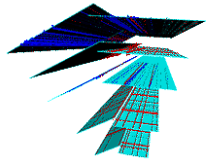

Layer 00
ISL
SVX II
64 cm


η=0
η=1
η=2
η=3
η=4
R=29 cm
ISL
Port Cards
SVX II
Layer 00
90 cm

CDF Data Flow



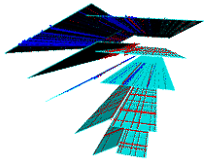
CDF English



Main Entry: ac.ro.nym
Pronunciation: 'a-kr&-"nim
Function: *noun*
Etymology: *acr- + -onym*
Date: 1943
: a word (as *NATO*, *radar*, or *snafu*) formed from the initial letter or letters of each of the successive parts or major parts of a compound term

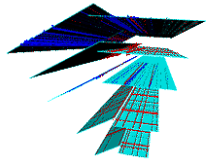
Main Entry: ab.bre.vi.a.tion
Pronunciation: &-"brE-vE-'A-sh&n
Function: *noun*
Date: 15th century
1 : the act or result of abbreviating
2 : a shortened form of a written word or phrase used in place of the whole <*amt* is an *abbreviation for amount*>

Overview of the Si DAQ



Slides of Si DAQ schematic and command path here.

Overview of the Si DAQ



Daq Components:

The SVX3D chip: Analog front end amplifies signal from 128 Si strips, stores charge on a pipeline of 46 capacitors (cells). Independant back end digitizes and transmits 8 bits of data and a data clock.

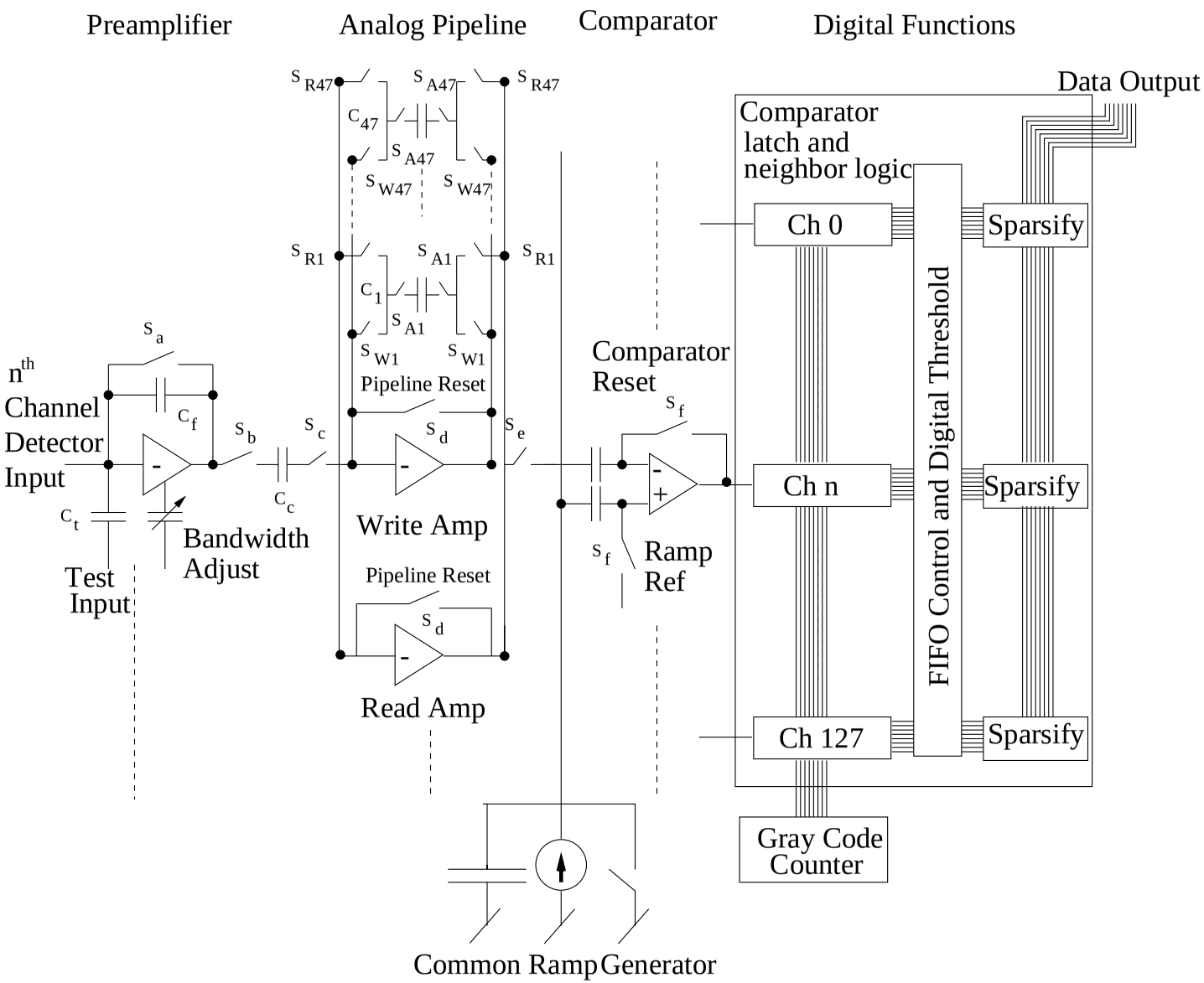
Compact Port Card (CPC): Transmits control signals from DAQ to SVX3D chips. Optically transmits 9 data bits to DAQ front-end.

Fibre Interface Board (FIB): Front-end of DAQ recieves optical readout from Si. Flash RAM used for programming and storing SVX3D control sequencies.

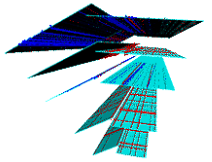
VME Readout Buffer (VRB): Common DAQ back-end for all CDF systems. Memory buffers for data to be collated by the CDF Hardware Event Builder (HEVB).

Silicon Readout Controller: Interface between CDF DAQ and Si DAQ systems. THE BRAIN.

The SVX3D Chip



The SVX3D Chip



Each chip reads out 128 strips. Chip Features:

A pipeline: A total of 46 cells. The pipeline depth is 42 cells depth = 42 × 132 ns between beam crossings = 5.5 μ secs propagation/processing time for L1 accept decision from CDF DAQ.

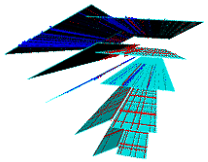
Deadtimeless 4 of the pipeline cells are dedicated to L1-accept buffers for *deadtimeless* operation.

A Seperate Back-End: Digital back-end is seperate from analog front end. Allows charge acquisition during digitization and readout. 8-bit ADC.

Dynamic Pedestal Subtraction: By delaying the start of the digitization counter until 30-40 strips have fired, an event by event pedestal subtraction is applied to the data.

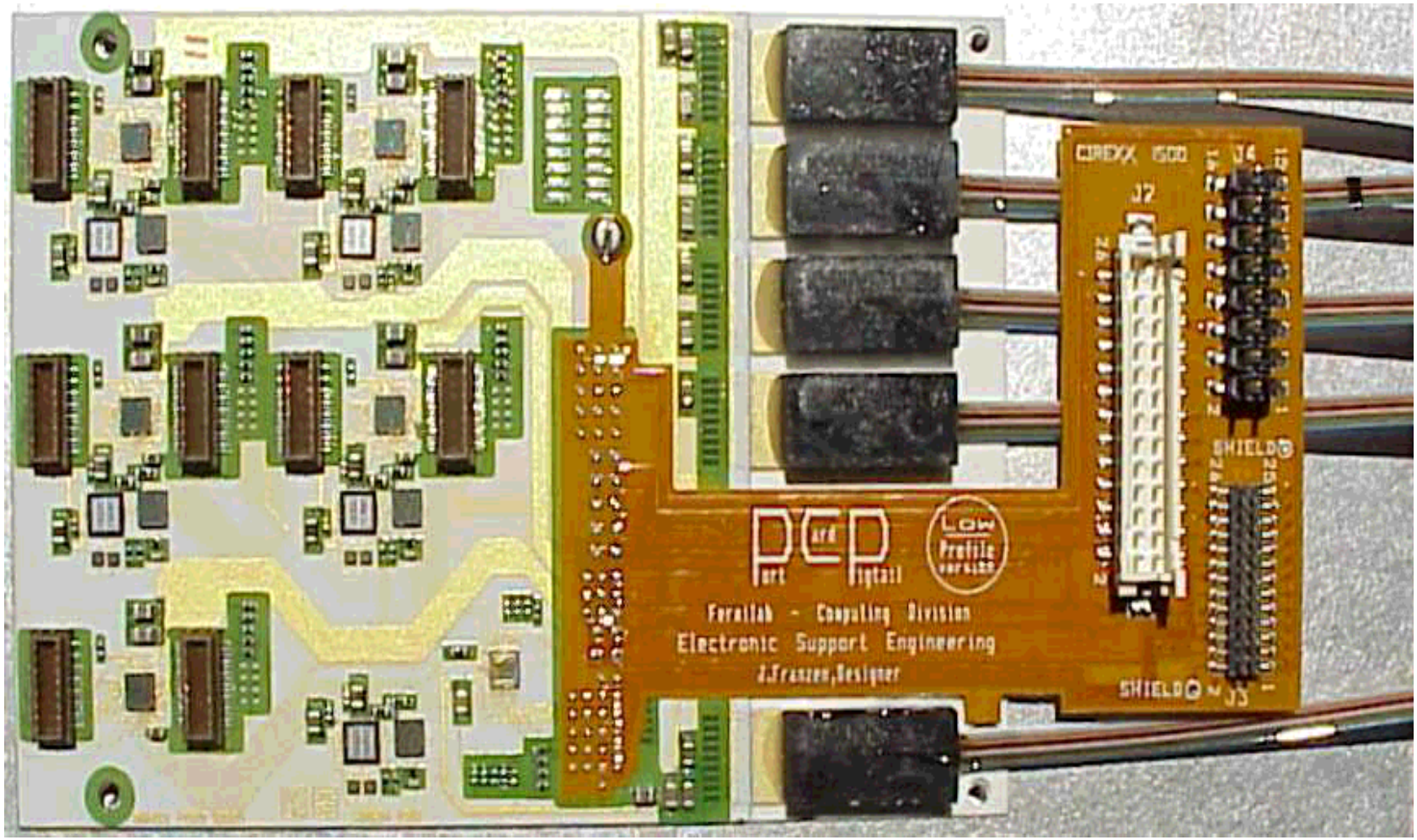
Programmable settings: 197 bits control operation. 128 channel masks, preamp band width settings, ADC ramp settings, ADC bandwidth, polarity settings, sparsification modes.

SVX3D in-situ



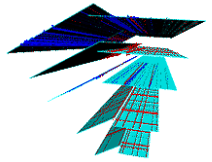
Show picture of Bert hanging barrel in the air and closup of vertical barrel to show chips on hybrids, hybrids connected to Silicon.

The Compact Port Card



5 Channels/CPC. SVXII CPCs readout 5 1/2 ladders = 44 chips. ISL CPCs readout 5x16chips/unit = 80 chips. 114 CPCs total in system

The Compact Port Card



Components of the CPC:

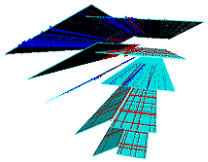
Transciever Chip: Converts low-voltage differential signals from DAQ to single ended. Differential reduces noise and signal degradation over long cables (76').

Digital Data Reciever (DDR): Decodes 5 bit commands into 10 SVX3D chip CMOS control signals + calibration voltages (4 bit Digital-to-Analog convertor) using a control.

Analog DDR: Regulates chip analog voltage (AVDD) for clean front-end operation.

Dense Optical Interface Module (DOIM): Converts differential 9 bit digital data from chip (8 data bits 1 Data Valid signal) into single ended input to a Laser Diode Array (LDA) which then transmits it to the DAQ front-end via a 9-bit parallel optical link.

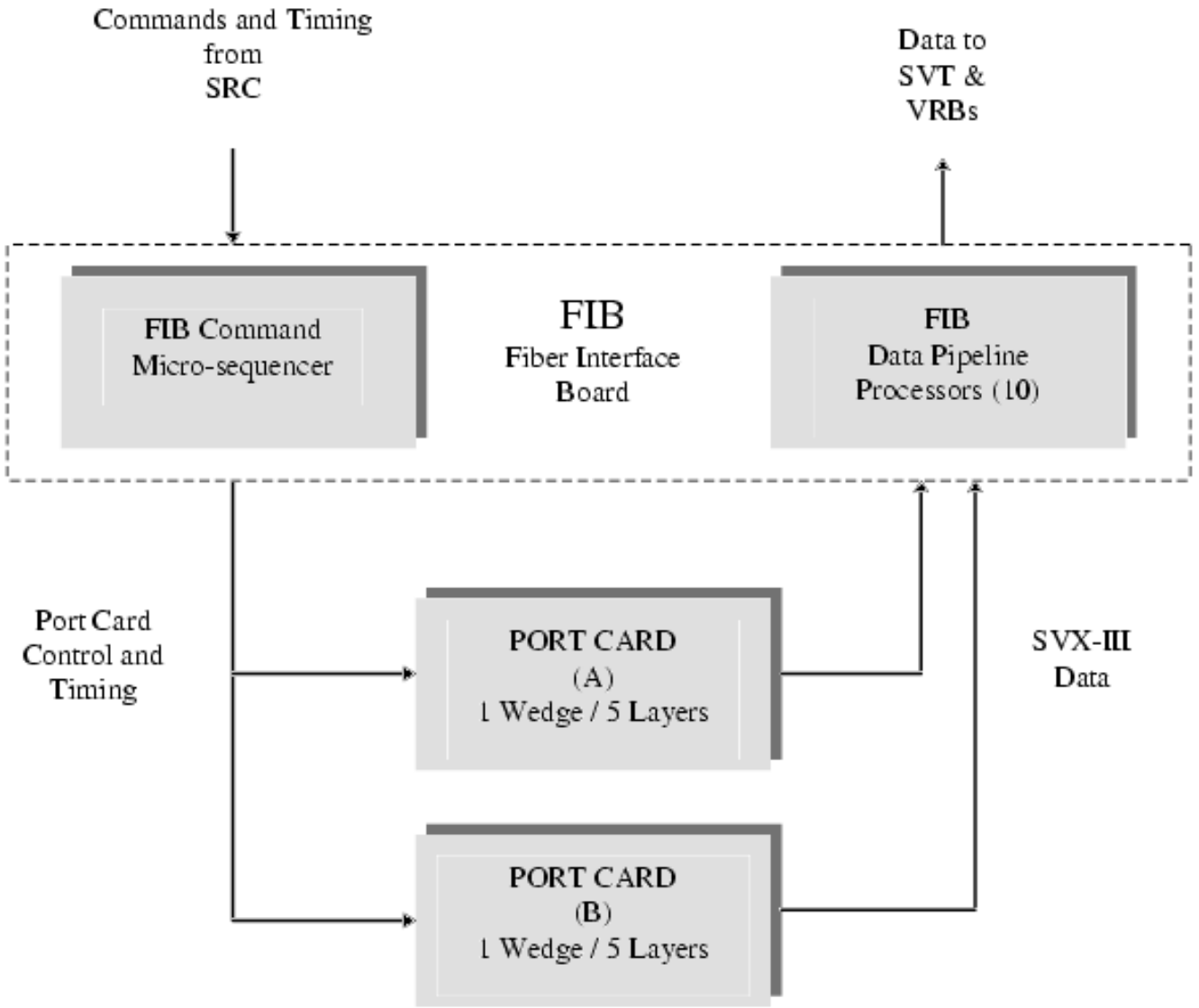
CPC in-situ



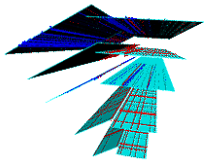
Show photos of the installation of the CPC rings and the final 3 barrels with all the CPCs on top.

Fiber Interface Board (FIB)

The FIB controls and recieves data from 2 CPCs via 10 input channels.



FIB Command Path



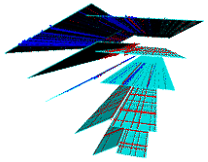
From SRC: Recieves CDF clocks from SRC the L1-accept and PRD2 (release tagged cell) chip signals, and commands to digitize, readout and reset preamp. Also recieves bunch crossing number.

To CPC: . Converts CDF clocks, L1A and PRD2 signals into chip-friendly format and transmits to CPC. *Microsequencer* synched to clocks from SRC converts digitize, readout and preamp reset commands from SRC into 5-bit encoded SVX3D command sequencies (programmable and storable in EPROMs) that are transmitted to the CPC.

From CPC: A transition module, OFTM with receiver DOIMS (RX-DOIM) convertes optical data from 10 CPC channels and transmits to FIB board.

To VRB/SVT: Data from all 10 CPC channels is collated and transmitted via 4 optical GLinks (GHz link) to the VRB and Silicon Vertex Trigger (SVT).

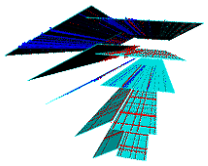
FIB Data Pipeline



Data Processing

- A FIB id word identifying Si and bunch crossing number are appended to the CPC data stream from each channel.
- A lookup table in RAM is used to subtract pedestals on a strip by strip basis from data if desired. Up to 4 sets of pedestal per strip can be subtracted determined by the chip state (quiescent, digitize, readout, ..)

VME Readout Buffer (VRB)



Si has special VRBs different from the calorimeter and D0 versions:

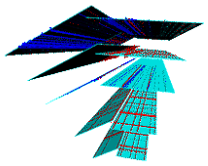
From SRC: Recieves bunch crossing number, expected pipeline cell id and buffer number from SRC every time a L1A is issued.

From FIB: Data from 10 FIB channels is read into the right buffer (4 read buffers/channel)

To CDF Hardware Event Builder: Data from 10 channels is scanned into a single output FIFO on receipt of a L2-accept to be by the CDF HEVB.

Data processing: Pipeline cell ids from each chip are checked for synchronization. Also checks bunch crossing numbers from each FIB channel. Strip occupancy histograms are stored on board.

Si Readout Controller (SRC)



To control the large data throughput and insure proper deadtimeless operation a special controller is used as an interface between CDF and Si DAQ:

From CDF Clock/Emulator: Recieves 53 MHz synch clock, RF clock and the accelerator bunch crossing structure. A master clock FPGA can emulate a programmed beam structure in standalone mode.

From CDF TS/Emulator: Recieves L1A and L2 decisions. Also has an onboard *TS Emulator*.

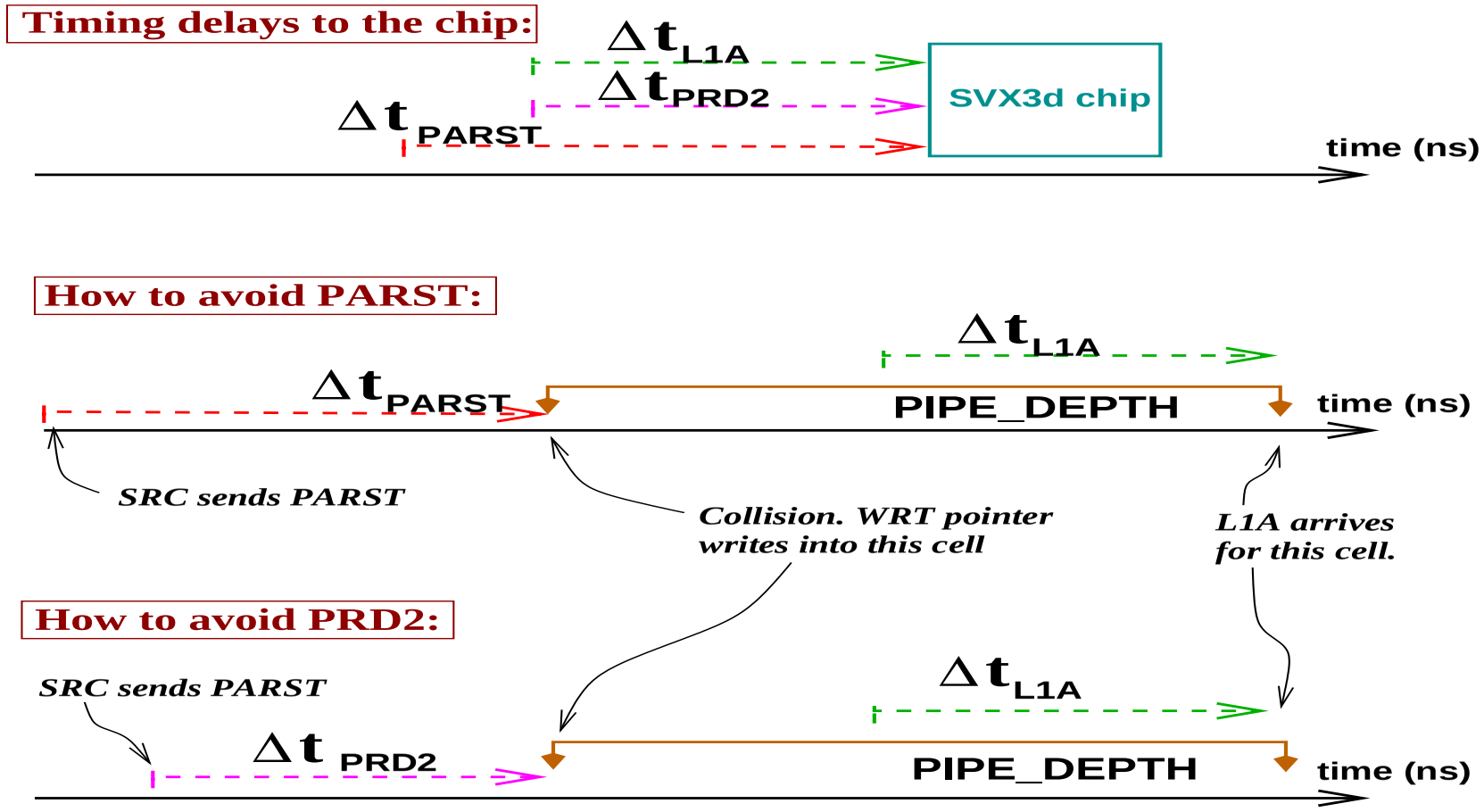
From VRBs: Recieves read/scan busy signals indicating VRB state. Throttles TS accordingly. Each VRB crate has one VRB Fanout module that recieves the SRC commands and sends it to all the VRBs on a specialized backplane.

To CDF TS/Emulator: Sends L1 done signal indicating VRBs are ready to recieve data. Otherwise TS is prevented from sending any more triggers.

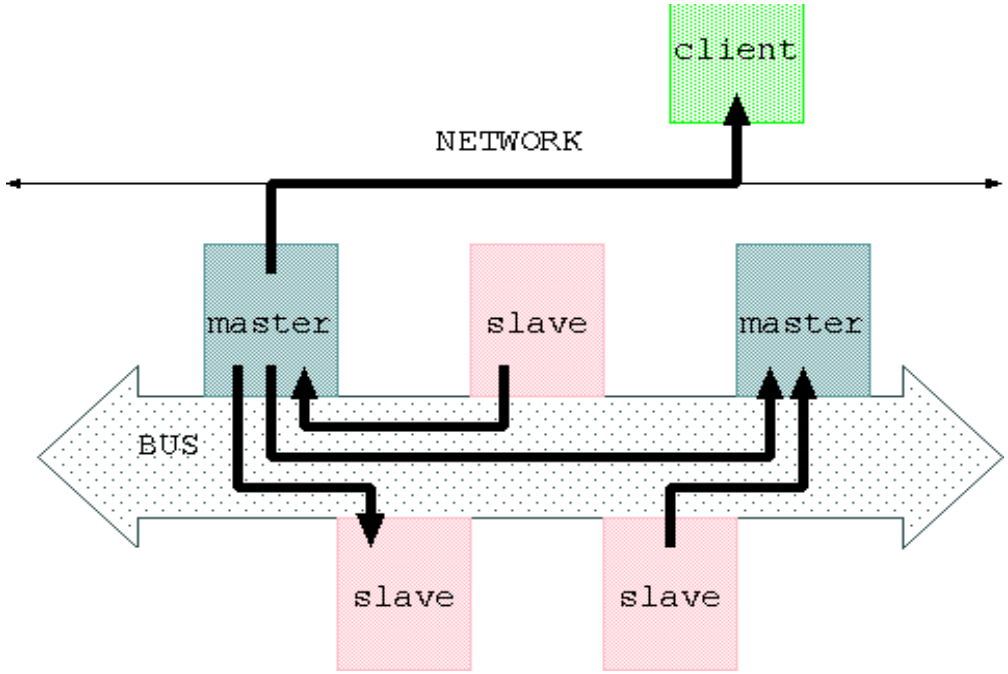
To FIBS: Sends L1A, PRD2, digitize, readout and preamp reset commands over GLinks to 8 Fib Fanout (FFO) modules which send them to the FIBs.

SRC and Preamp Resets

The SVX3D has an integrating preamp as input. It must be reset to insure collection of all the charge!. Only the SRC has knowledge of the triggers and beam structure. An example of the complicated timing logic implemented by the SRC:



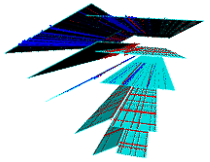
DAQ Control



Versa Module Europe (VME): Flexible open-ended bus system which makes use of the Eurocard standard introduced by Motorola, Phillips, Thompson, and Mostek in 1981.

VISION: (Versatile I/o Software Interface for Open-bus Networks) specifies a standard way to move data among entities connected by a bus and/or a network. Used to talk to VME boards connected by a VMEbus.

DAQ Control

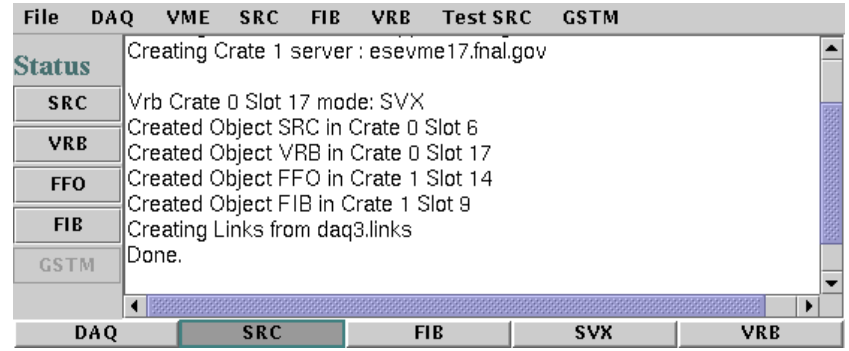


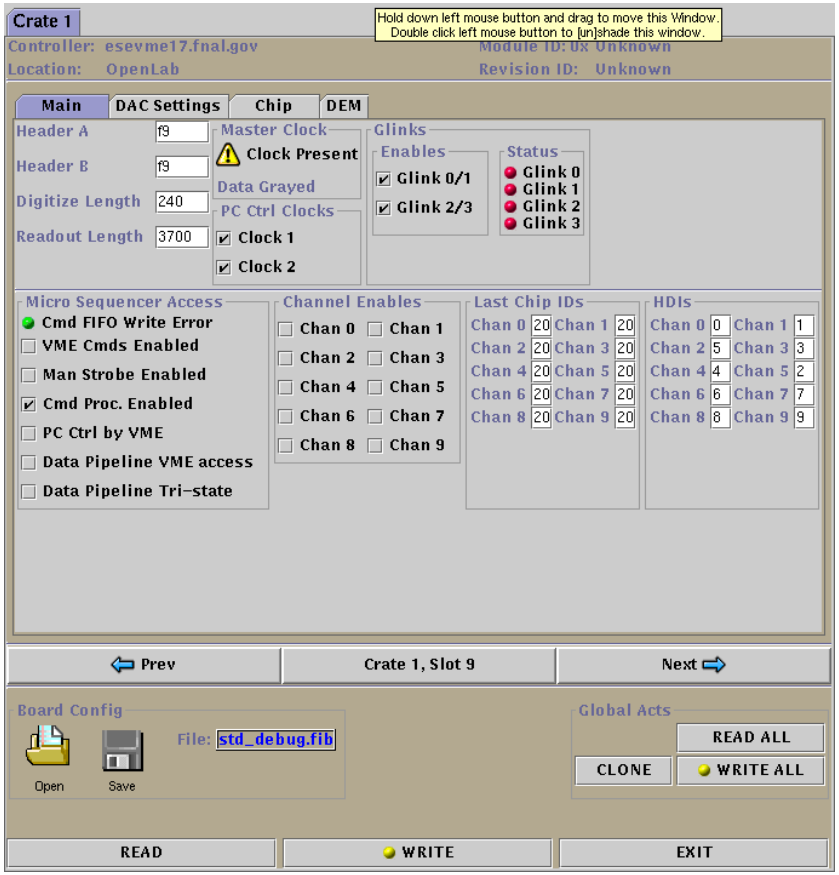
VxWorks: Real-time, UNIX-like portable operating system. Runs on VME controller boards (powerPC processors).

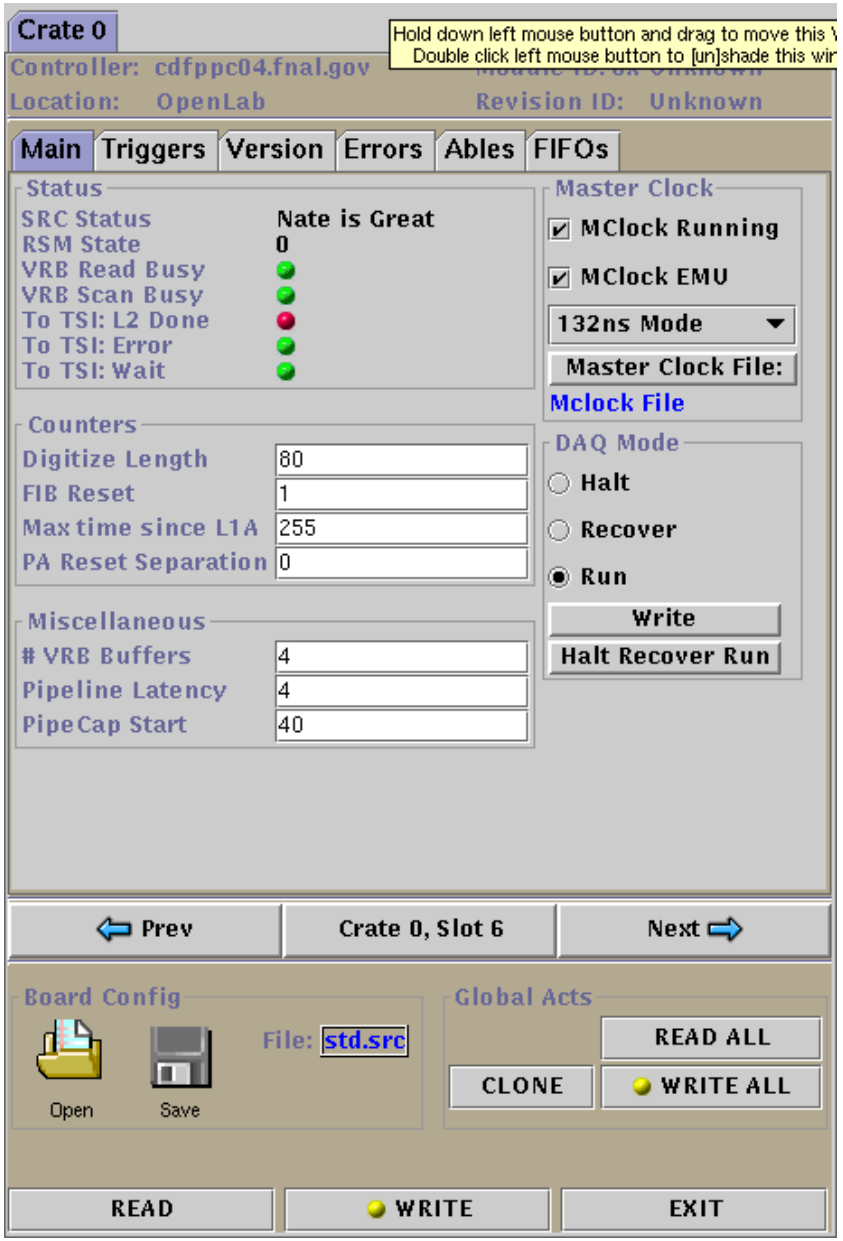
CORBA/ROBIN: The Common Object Request Broker Architecture is a standard framework allowing software objects to communicate with one another, no matter where they are located or who has designed them. ROBIN is FNAL's implementation of CORBA which supports remote procedure calls. Used by Client software to communicate with VME controller and subsequently the boards themselves.

SmartSockets: Commercial product which provides real-time publish-subscribe, multicast and message queuing. Used by CDF Run Control.

The JAVA Client interface

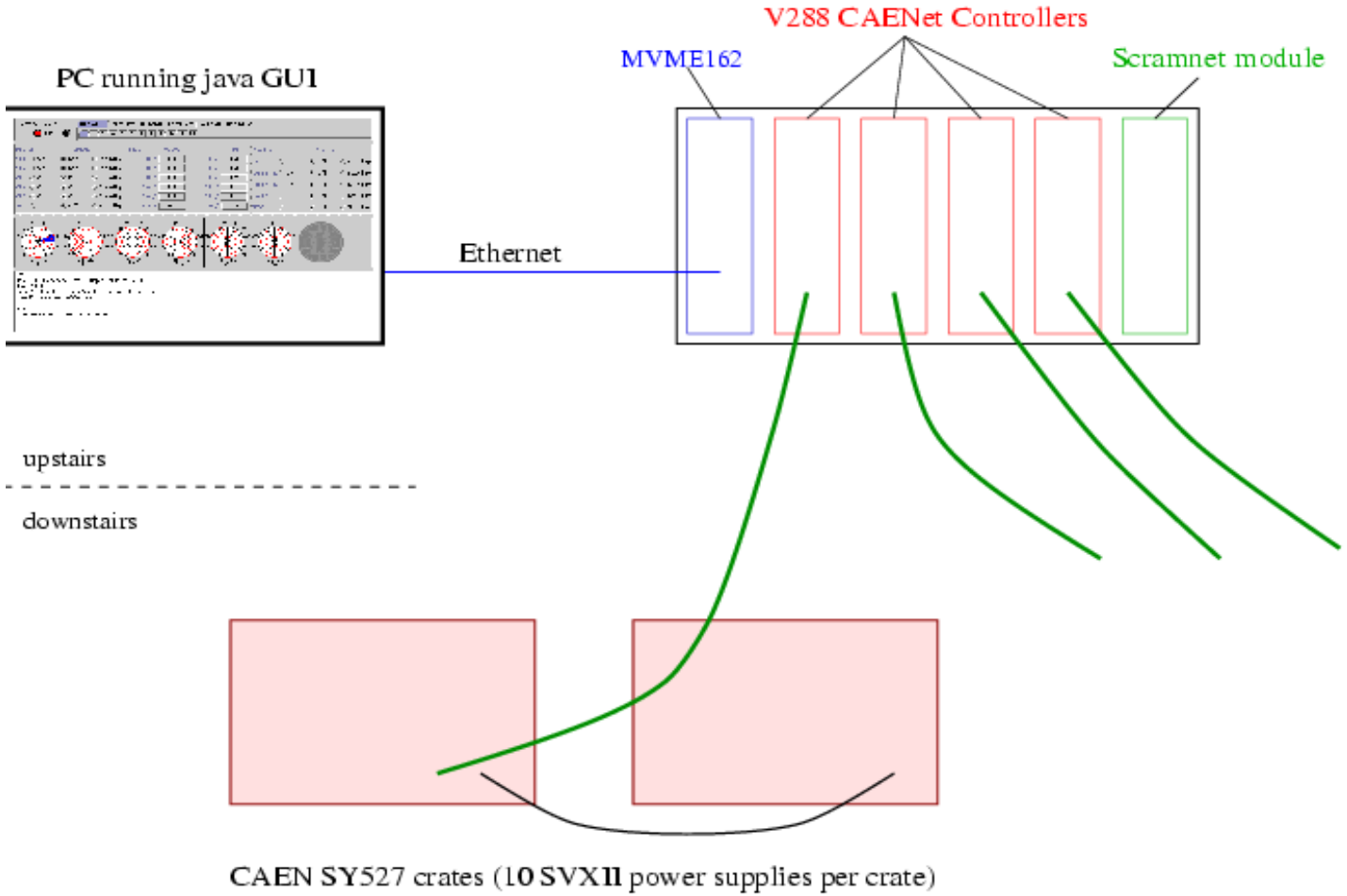




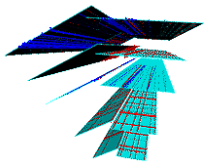


Si Power Control

Si power is also provided through a VME based DAQ system. Si Power communicates with FIBs using SmartSockets to initialize chips properly independant of CDF DAQ.



Integration with CDF/Si

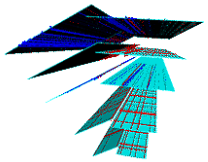


The Si DAQ was fully integrated with CDF DAQ before Si detector arrived in B0.

Data Emulator Module (DEM): 20 programmable data emulator boards were installed in the back of the FIB crate. Emulated read-all and sparsified data from chip. Used for testing data throughput, bit error rates, Glinks, TS-SRC-FIB-VRB path.

TestStands: 5 fully instrumented test-stands with the SRC emulating CDFCLK and TS were used to finalize SRC and FIB chip timing during all stages of production: hybrid $\rightarrow$ ladder $\rightarrow$ barrel and CPCs.

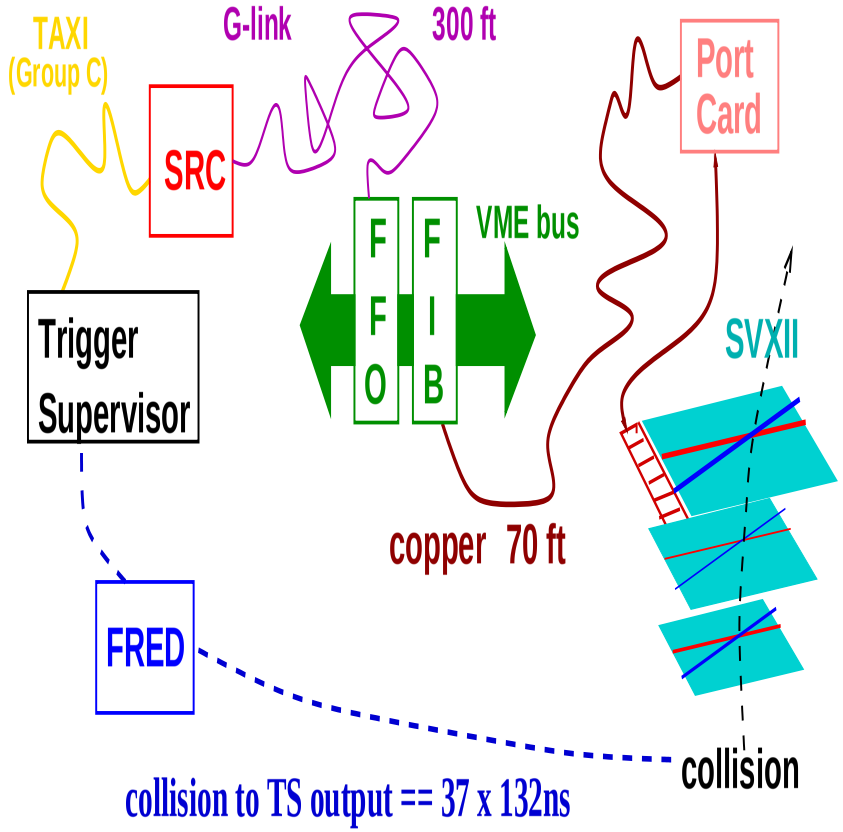
Si comes to CDF

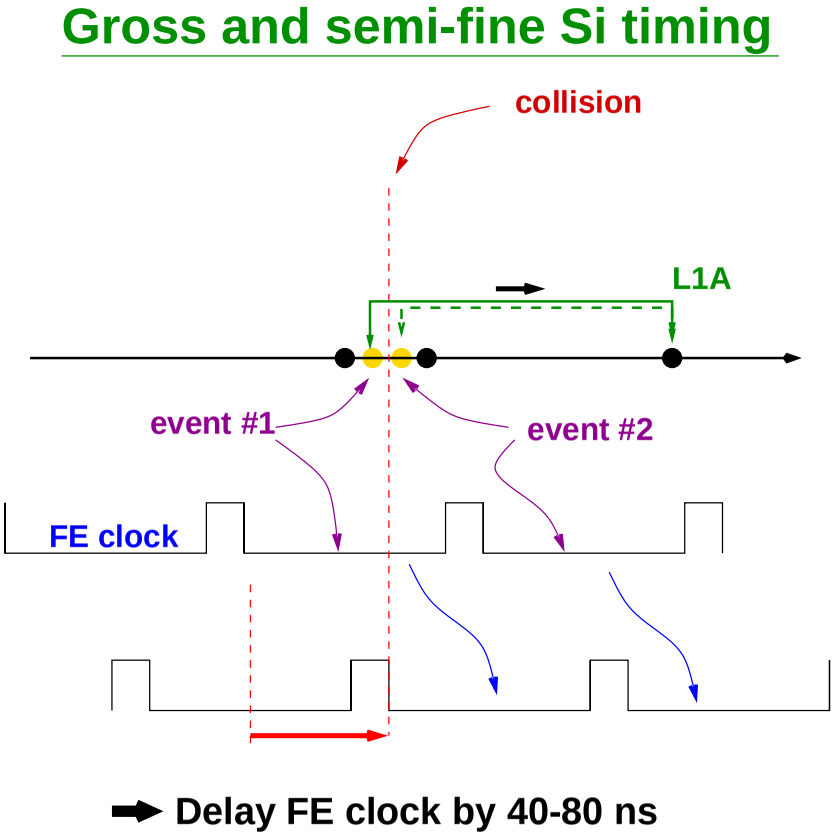


Photos of Si being hauled into CDF, plugging crew, plugged Si

Si Commisioning Timing in

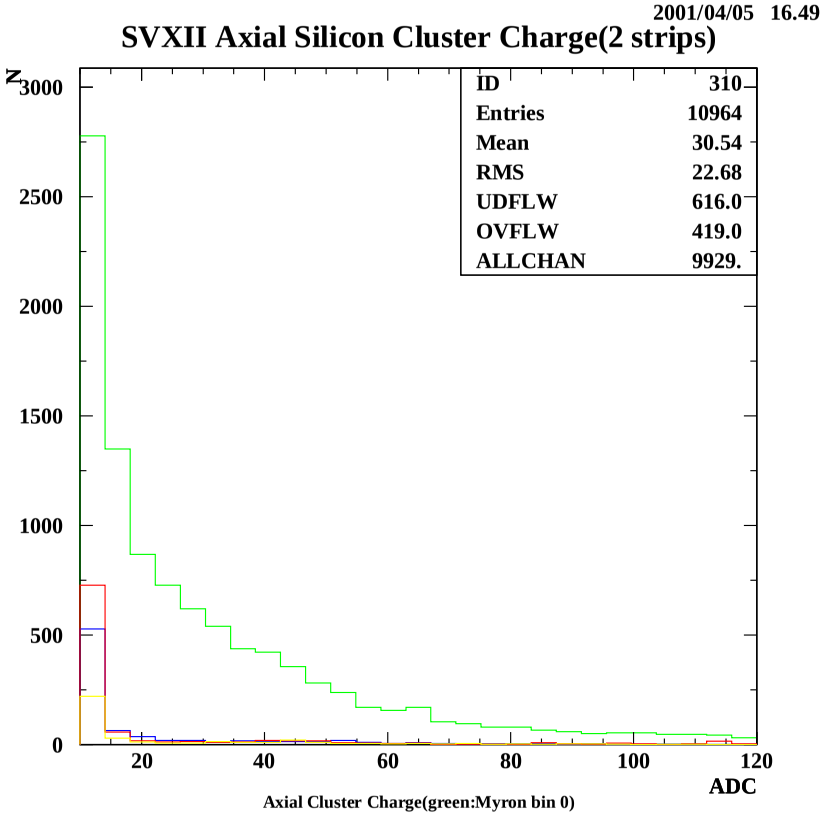
One of the first goals of the engineering and commisioning run was to make sure Si was synchronized with the rest of CDF and the accelerator. The SRC makes this possible:

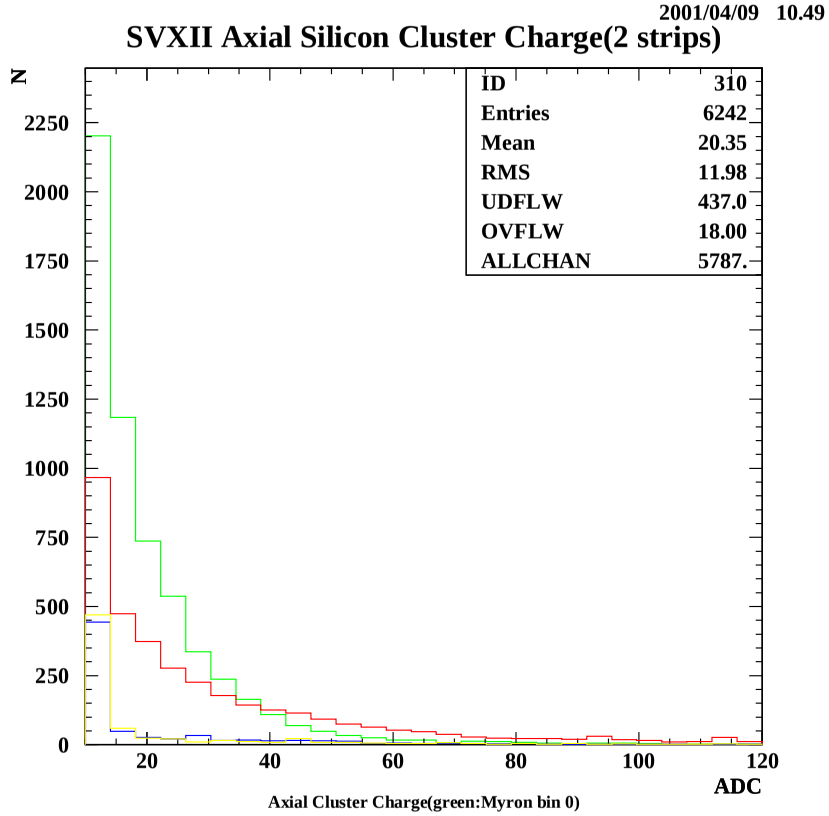




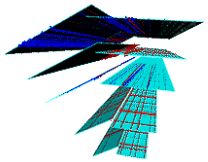
Right Bucket?

MYRON MODE: Send 4 L1A in row, before and after the true collision bucket. Look at charge clusters in each bucket





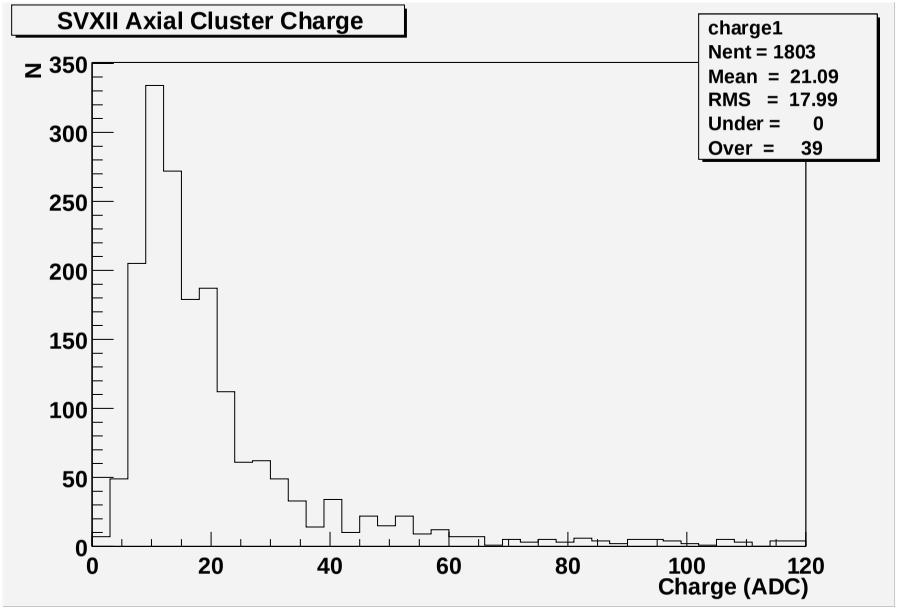
TRACKS!!!!

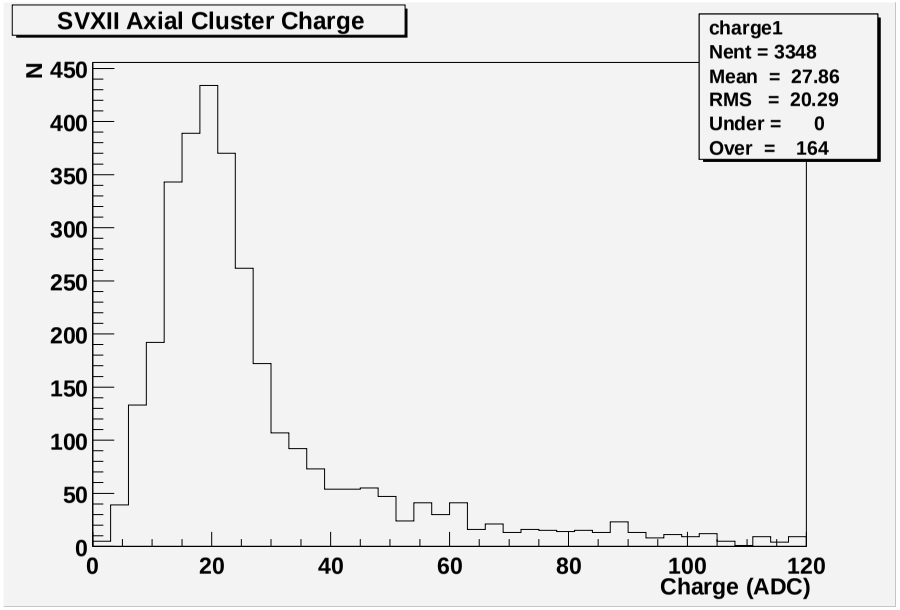


Put pictures of B4 tracks here. Stuff from Aaron too.

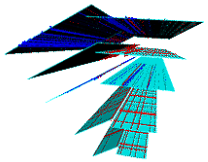
Integrating ALL charge?

Using hits on track look at Landau distributions as you scan within a 132 ns bucket:





Where are we now?



Problems with ISL cooling = no central barrel or layer 6 on the inner bulkhead of outer barrel. To be fixed next access :(

- All wedges are plugged in and have full DAQ instrumentation. 3/72 SVX 1/2 wedges have readout problems - not fully understood.
- Still missing some ISL/L00 power supplies.
- Intermittent problems with dropped bits on OFTMs. Problem understood.
- Currently cycling through all wedges testing and integrating. Few ladders with individual problems are getting expert attention.
- PHYSICS SOON!